Amendments to the Claims

1. (CURRENTLY AMENDED) A circuit ~~(200)~~ for transferring to a monitor clock domain ~~(180)~~ target events that occur in a target clock domain ~~(170)~~, the transfer circuit comprising:

a detector ~~(210)~~, in the target clock domain, configured to assert a target-domain event signal ~~(215)~~ each time the target event occurs;

a sending circuit ~~(220)~~, in the target clock domain, configured to change the value of a request signal ~~(150)~~ each time the target-domain event signal is asserted; and

a receiving circuit ~~(230)~~, in the monitor clock domain, configured to detect the change in value of the request signal, and to assert a monitor-domain event signal ~~(235)~~ once for each change in value detected.

2. (CURRENTLY AMENDED) The transfer circuit of claim 1, wherein:

the transfer circuit is adapted for use in a debug module ~~(140)~~ within an integrated circuit ~~(100)~~; and

the transfer circuit further comprises a monitor circuit ~~(240)~~ configured to assert a debug event ~~(245)~~ signal in response to the monitor-domain event signal.

3. (CURRENTLY AMENDED) The transfer circuit of claim 1, further comprising:

a second detector ~~(210)~~, in a second target clock domain ~~(170)~~, configured to assert a second-target-domain event signal ~~(215)~~ when a second target event occurs;

a second sending circuit ~~(220)~~, in the second target clock domain, configured to change the value of a second request signal ~~(150)~~ each time the second target-domain event signal is asserted; and

a second receiving circuit ~~(230)~~ in the monitor clock domain configured to detect the change in value of the second request signal, and to assert a second monitor-domain event signal ~~(235)~~ once for each change in value detected.

4. (CURRENTLY AMENDED) The transfer circuit of claim 3, further comprising:

a monitor circuit ~~(240)~~, in the monitor clock domain, configured to increment a first count ~~(445)~~ in response to the monitor-domain event signal, to increment a second count ~~(445)~~ in response to the second monitor-domain event signal, to hold a first target value ~~(455)~~, to produce a first trigger signal ~~(465)~~ by comparing the first count with the first target value, to hold a second target value ~~(455)~~, and to produce a second trigger signal ~~(465)~~ by comparing the second count with the second target value;

wherein the transfer circuit is adapted for use in a debug module ~~(140)~~ within an integrated circuit ~~(100)~~, and the monitor circuit is further configured to assert a debug signal ~~(245)~~ based on a signal selected from the first trigger signal, the second trigger signal, or a logical combination thereof.

5. The transfer circuit of claim 1, wherein the period of the target clock is at least the sum of the period of the monitor clock plus the set up time required by the receiving circuit.

6. (CURRENTLY AMENDED) A circuit ~~(400,500)~~ for transferring to a monitor clock domain ~~(180)~~ target events that occur in a target clock domain ~~(170)~~, the transfer circuit comprising:

a counter ~~(410)~~, in the target clock domain, configured to generate an incremental count ~~415~~ of occurrences within a time period of the target event and, in response to a transfer signal ~~(525)~~, to transfer the incremental count and clear the incremental count;

a sending register ~~(420)~~, in the target clock domain, configured to load the incremental count in response to the transfer signal, and to hold the incremental count, wherein the time period that the counter generates the incremental count includes the time period during which the sending register holds the incremental count;

a request sending circuit ~~(220)~~, in the target clock domain, configured to change the value of a request signal ~~(150)~~ in response to the transfer signal;

a request receiving circuit ~~(230)~~, in the monitor clock domain, configured to

detect the change in value of the request signal and, in response thereto, to generate a receive signal ~~(535)~~;

a receiving register ~~(430, 530)~~, in the monitor clock domain, configured to load the incremental count from the sending register in response to the receive signal;

an acknowledgement sending circuit ~~(470)~~, in the monitor clock domain, configured to change the value of an acknowledgement signal ~~(475)~~ in response to the receive signal;

an acknowledgement receiving circuit ~~(480)~~, in the target clock domain, configured to detect the change the value of the acknowledgement signal and, in response thereto, to assert a target-domain acknowledgement signal ~~(524)~~; and

a control circuit ~~(520)~~, in the target clock domain, configured to generate the transfer signal when the incremental count in the counter is non-zero and the target-domain acknowledgement signal has been asserted for each change in value of the request signal.

7. (CURRENTLY AMENDED) The transfer circuit of claim 6, wherein the receiving register ~~(530)~~ is further configured to assert a monitor-domain event signal ~~(235)~~ when the incremental count in the receiving register is non-zero and to decrement the incremental count each time the monitor-domain event signal is asserted.

8. (CURRENTLY AMENDED) The transfer circuit of claim 6, further comprising:

a monitor circuit ~~(240)~~, in the monitor clock domain, configured to add the incremental count to an event count ~~(445)~~.

9. (CURRENTLY AMENDED) The transfer circuit of claim 8, wherein:

the transfer circuit is adapted for use in a debug module ~~(140)~~ within an integrated circuit ~~(100)~~; and

the monitor circuit is further configured to hold a target value ~~(455)~~, to compare the event count with the target value, and to assert a debug signal ~~(245)~~ based thereon.

10. (ORIGINAL) A circuit for transferring to a monitor clock domain target events that occur in a target clock domain, the transfer circuit comprising:

means, in the target clock domain, for detecting occurrences of the target event and for asserting, in response thereto, a target-domain event signal;

means, in the target clock domain, for changing the value of a request signal response to the target-domain event signal;

means, in the monitor clock domain, for receiving the request signal and for asserting a monitor-domain event signal in response to the value of the request signal changing.

11. (ORIGINAL) The transfer circuit of claim 10, wherein:

the transfer circuit is adapted for use in a debug module within an integrated circuit; and the transfer circuit further comprises means for triggering a debug event in response to the monitor-domain event signal.

12. (ORIGINAL) The transfer circuit of claim 10, wherein:

the value of the request signal changes each time the target-domain event signal is asserted; and the period of the target clock is at least the sum of the period of the monitor clock plus the set up time required by the receiving means.

13. (ORIGINAL) The transfer circuit of claim 10, further comprising:

means, in the target domain, for counting occurrences of the target event within a time period, thereby generating an incremental count, and, when enabled, for transferring a non-zero incremental count and resetting the incremental count;

means, in the target domain, for holding the incremental count received from the counting means, wherein the time period during which the counting means counts includes the time period during which the holding means holds the incremental count; and

means, in the monitor domain, for responding to the change in value of the request signal by receiving the incremental count from the holding means and by changing the value of an acknowledgement signal; and

means, in the target domain, for disabling the transfer of a non-zero incremental count until the acknowledgement signal changes value;

wherein the value of the request signal changes each time that a non-zero incremental count is transferred.